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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/758,675	01/11/2001	Klaus Gloeckler	10191/1639	9544

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	8

DATE MAILED: 12/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/758,675	GLOECKLER ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The replacement drawing of Figure 2 was received on 17 November 2003. The drawing is approved however the handwriting in the drawing is difficult to read and the drawing is not acceptable as a replacement sheet.

New corrected drawings are required in this application because the drawing labels in Figure 2 are handwritten and illegible in places. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Response to Amendment

2. Applicant's arguments with respect to claims 1, 3-10 and 12 have been considered but are moot in view of the new ground(s) of rejection. Note: Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Claim Objections

3. Claims 1 and 3-9 objected to because of the following informalities: claim 1

recites "activating the JTAG interface of the microprocessor with a test routine that is executable on the microprocessor and then transmitted to the JTAG interface". The Examiner asserts that no action was carried out prior to the then clause; hence it is not clear after what action the test routine is transmitted. The Examiner assumes the Applicant intended: --activating the JTAG interface of the microprocessor with a test routine that is executable on the microprocessor and **transmitting the test routine** to the JTAG interface--.

Claims 3-9 depend from claim 1; hence inherit the deficiencies of claim 1.

Appropriate correction is required.

4. Claim 12 is objected to because of the following informalities: claim 12 recites, "enabling input of defined values by an external device". The examiner recommends the following to correct the grammatical error: --enabling input**s** of defined values by an external device--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. Claims 1 and 3-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites "activating the JTAG interface of the microprocessor with a test routine that is executable on the microprocessor and then transmitted to the JTAG interface".

The Examiner asserts that no action was carried out prior to the then clause; hence it is not clear after what action the test routine is transmitted rendering the language incomprehensible and indefinite. The Examiner assumes the Applicant intended: -- activating the JTAG interface of the microprocessor with a test routine that is executable on the microprocessor and **transmitting the test routine** to the JTAG interface--.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3-8, 10 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Argade, Pramod Vasant et al. (US 5724505 A, hereafter referred to as Argade).

35 U.S.C. 102(b) rejection of claims 1 and 10.

Argade teaches method for activating a microprocessor (processor core 12 in Figure 1 of Argade is a microprocessor since it is part of the digital processor of Figure 1, also see col. 4, lines 1-3 and col. 1, lines14-22 in Argade) arranged as a part of a microcontroller (col. 4, lines 1-3 and col. 1 in Argade teach that the circuit of Figure 4 is a digital processor and col. 1, lines14-22 in Argade teach that the digital processor can be replaced with a microcontroller), within a framework of a boundary scan test

procedure as set forth in IEEE standard 1149 using a JTAG interface of the microprocessor (See JTAG Interface 24 in Figure 1 of Argade; also see col. 2, lines 7-30 in Argade which teaches that the JTAG Interface 24 in Figure 1 of Argade is within the framework of a boundary scan test procedure as set forth in IEEE standard 1149), comprising the step of: activating the JTAG interface of the microprocessor with a test routine that is executable on the microprocessor and **transmitting the test routine** to the JTAG interface (col. 5, lines 14-30 of Argade teach that the JTAG interface of the microprocessor, processor core 12 in Figure 1 of Argade, is activated to transmit and receive signals via lines 42 and 46 in Figure 1 when the program trace test routine has been transmitted to the JTAG Interface 24 via line 38; hence Argade teaches activating the JTAG interface 24 of Figure 1 of the microprocessor, processor core 12, to transmit and receive signals via lines 42 and 46 with a program trace test routine that is executable on the microprocessor and **transmitting the** program trace **test routine** to the JTAG interface); wherein I/O ports of the microprocessor are connected to pins of the JTAG interface, and a data-in pin of the JTAG interface is activated using the test routine via the I/O ports (Note: line 46 in Figure 1 is a data in line, which is connected to the JTAG port data-in pin and **transmitting the** program trace **test routine** to the JTAG interface activates the JTAG port data-in pin by activating signal line 46, furthermore, the JTAG port data-in pin is also the data-in pin of the JTAG interface, hence Argade teaches the I/O ports of the microprocessor, processor core 12, are connected to pins of the JTAG interface 24, and a data-in pin of the JTAG interface is activated using the test routine via the I/O ports).

35 U.S.C. 102(b) rejection of claim 3.

Argade teaches performing at least one of a setting operation and a reading operation with respect to the pins of the JTAG interface, the setting operation including inputting a stipulated test sequence in the test routine to the pins of the JTAG interface (col. 3, lines 35-40 of Argade teach trace recording hardware receives, via an instruction type line, data indicative of instruction types executed by the processor core and also receives, via an inter-module bus, data indicative of program addresses corresponding to the instruction types received via the instruction type bus.), and the reading operation including reading a sequence of output values at the pins of the JTAG interface corresponding to the stipulated test sequence in the test routine (claim 1 in Argade teaches output means for sending out said compressed program trace via the serial port).

35 U.S.C. 102(b) rejection of claim 4.

Argade teaches causing the test routine to provide a test data stream to the JTAG interface within the framework of the boundary scan test procedure (Argade teaches activating the JTAG interface 24 of Figure 1 of the microprocessor, processor core 12, to transmit and receive signals via lines 42 and 46 with a program trace test routine that is executable on the microprocessor and **transmitting the** program trace **test routine** to the JTAG interface; Note: Input line 46 is for a test data stream).

35 U.S.C. 102(b) rejection of claim 5.

Argade teaches switching the I/O ports of the microprocessor to transmit the test routine for a predefined duration to output ports and to high (col. 5, lines 14-30 of Argade teach **transmitting the** program trace **test routine** to the JTAG interface; Note: a test routine has a predefined duration); and measuring levels present at an interface of the microcontroller (JTAG boundary scan circuitry is composed of output scan elements used to measure the level at the output of a circuit).

35 U.S.C. 102(b) rejection of claim 6.

Argade teaches switching the I/O ports of the microprocessor to input ports to enable reception of values from the pins of the JTAG interface generated by the test routine for a predefined duration (Argade teaches activating the JTAG interface 24 of Figure 1 of the microprocessor, processor core 12, to transmit and receive signals via lines 42 and 46 with a program trace test routine that is executable on the microprocessor and **transmitting the** program trace **test routine** to the JTAG interface; Note: Input line 46 is for a test data stream; Note: a test routine has a predefined duration); and applying defined values to an interface of the microcontroller to transmit the stipulated test sequence to the microcontroller (line 46 in Figure 1 is used to transmit test data, i.e., the stipulated test sequence, to the microcontroller).

35 U.S.C. 102(b) rejection of claim 7.

Argade teaches reading values present at the pins of the JTAG interface via the I/O

ports of the microprocessor; and storing the values present at the pins of the JTAG interface in a memory area of the microcontroller (col. 2, lines 22-26 in Argade teach test instructions via the JTAG port are shifted into the digital processor on-chip memory).

35 U.S.C. 102(b) rejection of claim 8.

Argade teaches reading out the values present at the pins of the JTAG interface and stored in the memory area via the interface of the microcontroller (col. 2, lines 22-26 in Argade teach the test results executed by the digital processor are scanned out through a JTAG port test data out (TDO) pin after the digital processor completes its operation).

35 U.S.C. 102(b) rejection of claim 12.

Argade teaches a JTAG port 44 and Interface 24 in Figure 1 of Argade for an interface to external devices, the interface enabling output levels present at the interface to be measured and enabling input of defined values by an external device.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Argade, Pramod Vasant et al. (US 5724505 A, hereafter referred to as Argade) in view of Margolis, Donald L. et al. (US 5357432 A, hereafter referred to as Margolis).

35 U.S.C. 103(a) rejection of claim 9.

Zuraski, substantially teaches the claimed invention described in claims 1 and 3-8 (as rejected above).

However Argade, does not explicitly teach the specific use of the microcontroller taught in the Zuraski patent **for a motor vehicle**.

Margolis, in an analogous art, teaches a microcontroller for use in a sensing system for a motor vehicle (col. 4, lines 60-68, Margolis). The Examiner asserts that it would be obvious to use the microcontroller taught in the Argade patent since that is what a microcontroller is designed for. One of ordinary skill in the art at the time the invention was made would have been highly motivated to use the microcontroller taught in the Argade patent in a motor vehicle because the microcontroller taught in the Argade patent has the added feature of Built-In Self-Test (BIST) logic which provides the ability

to test for circuit integrity and to repair circuit failures to maintain circuit integrity (see Abstract, Argade).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Argade with the teachings of Margolis by including use of the microcontroller taught in the Argade patent in a motor vehicle. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the microcontroller taught in the Argade patent in a motor vehicle would provide the opportunity to test for circuit integrity and to repair circuit failures to maintain circuit integrity (see Abstract, Argade).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bock, Robert et al. (US 5434804 A) teaches microprocessors and microcontrollers provided with a test control capability.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres, PhD
Art Unit 2133